REMARKS

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested. Claims 1-14 are pending in this application. No claims are amended herein. No claims have been allowed.

Claim Rejections – 35 U.S.C. § 102

Claims 1-2, 4-6, 8-9 and 11-13 stand rejected under 35 U.S.C. §102(b) as being anticipated by Gibson (U.S. Patent No. 6,274,896).

Gibson (abstract, cover figure and title) teaches a field effect transistor device with a folded (i.e., serpentine) gate electrode 16a/16b. The Examiner in particular refers to Gibson at Fig. 2 as teaching a field effect transistor device having a surface of a channel region below gate electrode 16 as being corrugated.

Applicant's response in the main is that each and every element within applicant's invention as disclosed and claimed within applicant's independent claims 1, 4-5, 8 and 11-12 is not taught within Gibson.

The key element of applicant's claimed invention is that at least one of: (1) an interface of a channel region covered by a gate electrode; and (2) a surface of the gate electrode, is corrugated. The corrugation is clearly shown in applicant's Fig. 1 which is a schematic perspective-view diagram and in applicant's Fig. 8 which is a schematic cross-sectional view diagram. In Fig. 1 in particular, corrugation of an entire active region 10' is shown. This includes source/drain regions 10a and 10b, as well as a channel region defined therebetween and beneath gate electrode 14. The surface of the gate electrode 14 is also clearly corrugated.

While the Examiner asserts that Gibson at Fig. 2 teaches a field effect transistor device with a surface of a channel region beneath gate electrode 16 as corrugated, applicant does

not believe that such a feature of Gibson's invention is discernable from Fig. 2. Unlike applicant's schematic perspective-view diagram of Fig. 1 and schematic cross-sectional diagram of Fig. 8, Gibson's Fig. 2 is a plan-view diagram that shows a disposition of a serpentine gate electrode 16 with respect to interdigitated source/drain regions 18 and 20. Gibson's plan-view diagram of Fig. 2 does not show any explicit topography to a surface of gate electrode 16. Nor clearly does Gibson's schematic plan-view diagram show any topography of an interface of a channel region covered by Gibson's gate electrode 16.

A better indication of a corrugation of a top surface of a gate electrode or an interface of a channel region covered by the gate electrode may be discerned from Gibson's Figs. 3a and 3b, which are in turn cross-sectional diagrams that correspond with Gibson's Fig. 1. In Fig. 3a and Fig. 3b, gate electrodes are designated as reference numerals 16a and 16b, channel regions are designated as reference numeral 22 (col. 3, line 30 to col. 4, line 5). In Fig. 3a and Fig. 3b, gate electrodes 16a and 16b clearly do not have a corrugation of a surface thereof. Rather upper surfaces of gate electrodes 16a and 16b are flat. In addition, an interface of a channel region 22 beneath a gate electrode 16a or 16b also does not have a corrugation. It similarly is also flat.

"A claim is anticipated only if each and every element set forth in the claim is found, either expressly of inherently described, in a single prior art reference." MPEP 2131 (citing *Verdegaal Bros. v. Union Oil Co. of California* (citation omitted)).

Gibson apparently does not teach a corrugation of at least one of: (1) a surface of a gate electrode; and (2) an interface of a channel region beneath the gate electrode, as claimed within applicant's claims 1, 4-5, 8 and 11-12. Rather Gibson teaches a surface of a gate electrode as flat and an interface of a channel region beneath the gate electrode also as flat. Since the corrugation of a surface of a gate electrode or an interface of a channel region therebeneath is an element of applicant's invention as claimed within claims 1, 4-5, 8 and 11-12

and the same is clearly absent within Gibson, applicant asserts that claims 1, 4-5, 8 and 11-12 may not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by Gibson. Since the remaining claims within the foregoing rejections are dependent upon claim 1 or claim 8 and carry all of the limitations of claim 1 or claim 8, applicant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by Gibson.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of claims 1- 2, 4-6, 8-9 and 11-13 under 35 U.S.C. § 102(b) as being anticipated by Gibson be withdrawn.

Claim Rejections – 35 U.S.C. § 103

Claims 3, 7, 10 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gibson.

The foregoing claims are directed towards numeric limitations pertinent to: (1) periodicity of corrugation within applicant's invention; and (2) thickness of applicant's gate electrode. The Examiner predicates obviousness of these claimed limitations upon applicant's absence of a disclosure that any of the foregoing numeric limitations is critical.

In response, applicant predicates patentability of applicant's claims 3, 7, 10 and 14 upon their dependence upon either claim 1 or claim 8.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of claims 3, 7, 10 and 14 be withdrawn.

Response to Arguments

In the Response to Arguments at page 3 of the office action made FINAL, the Examiner asserts that "the channel in the [Gibson] reference is, in fact, corrugated (see col. 4, lines 10-12)." The Examiner further asserts that "the top surface of [Gibson's] gate is corrugated, also (see figure 2)."

With the Examiner's foregoing assertions applicant respectfully disagrees.

First, Gibson at col. 4, lines 10-12 teaches "[a]n elongate source conductor 26 at least partially overlies the source 18 and the serpentine channel 22." Nowhere within the portion of Gibson as cited by the Examiner does Gibson apparently teach that any structure within Gibson's field effect transistor device is formed with a corrugated surface. More particularly, Gibson at col. 4, lines 10-12 does not teach at least one of: (1) an interface of a channel region covered by a gate electrode; and (2) an upper surface of the gate electrode, being corrugated. Rather Gibson at col. 4, lines 10-12 clearly teaches that a channel in plan view beneath a gate electrode 16a/16b is clearly formed in a serpentine shape since the gate electrode 16a/16b is formed in serpentine shape.

A serpentine shape in plan view of a channel is clearly not identical with: (1) a corrugation of an interface of the channel with a gate electrode; or (2) a corrugation of a surface of the gate electrode.

Second, while Gibson at figure 2 does in fact teach a pair of gate electrodes 16a and 16b, neither of the pair of gate electrodes 16a and 16b has a corrugated surfaces as would otherwise be clearly illustrated within Fig. 2. Rather Gibson at Fig. 2 illustrates and teaches that each of Gibson's gate electrodes is formed with a flat surface.

A flat surface in cross-sectional illustration of a gate electrode is clearly not identical to a corrugated surface in cross-sectional illustration of a gate electrode.

In light of the foregoing responses, applicant continues to assert that each and every element within applicant's invention as disclosed and claimed within claims 1, 4-5, 8 and 11-12 is not taught within Gibson as cited by the Examiner. Absent is a teaching of at least one of: (1) an interface of a channel region with a gate electrode; and (2) a surface of the gate electrode, being formed corrugated. In light of the foregoing assertion, applicant respectfully requests that the Examiner's rejections of applicant's claims 1, 4-5, 8 and 11-12 under 35 U.S.C. § 102(b) as being anticipated by Gibson be withdrawn.

Other Considerations

The Examiner has cited no additional prior art of record not employed in rejecting applicant's claims to applicant's invention. No fee is due as a result of this response.

SUMMARY

Applicant's invention as disclosed and claimed within claims 1, 4-5, 8 and 11-12 is directed towards a field effect transistor device and a method for fabricating the field effect transistor device. The field effect transistor device and the method provide that at least one of: (1) an interface of a channel region covered by a gate electrode; and (2) a surface of the gate electrode, is corrugated. The foregoing elements of applicant's claimed invention are absent from the art employed in rejecting applicant's claims to applicant's invention.

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CONCLUSION

On the basis of the above remarks, favorable reconsideration of this application, and its early allowance, are respectfully requested.

Any inquiries relating to this or previous communications pertaining to this application may be directed towards the undersigned attorney at 248-540-4040, at the Examiner's convenience.

Respectfully submitted,

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